Digital Integration

Introduction

When integrating the digital part of modern electronic systems, various technical and financial criteria must be considered. Over 10 years of ASIC experience have shown that no one methodology can meet all requirements at the same time. TEMIC's experience at proposing the most appropriate solution to its customers has resulted in long-term partnerships. Our customers/partners have themselves experienced several ways of completing ASICs, from the use of heavy internal investment with their own design centers, to full sub-contracting to ASIC vendors from product specifications.

Know-how protection, engineering workload management and evolution of merchant CAD tools have been key factors in the evolution of the preferred solutions.

The border between the in-house skills of equipment manufacturers and those of semiconductors makers has evolved: high level behavioral description, such as VHDL, has become the most appropriate language for users to bridge the gap between system description and physical implementation. At the other end of the scale, submicron electronics and faster digital systems have revealed new challenges to cope with the electrical behavior of signals, both on and outside the chip. For instance, clock or signal skews, cross-talks, noise, electromagnetic emission or susceptibility have become the main drivers of first-pass yields in design.

Testing of large integrated systems, sometimes including processor cores, is also a matter of trade-offs between circuit cost, development time and safety operation. New generations of programmable devices such as CPLD or FPGA have also appeared, offering unbeatable flexibility and development time, but with additional cost, sourcing, logistics, and reliability considerations.

In addition to the extensive experience of our designers, TEMIC has developed an unrivalled choice of ASIC solutions offering the best trade-off in development or production cost, flexibility or performance.

Our solutions are also compatible with previous choices or vendor policies from our clients. On top of our proven capacity to deliver high-quality silicon devices in volume, we are recognized for helping our customers to secure their present or future supplies, while remaining competitive for the lifetime of their systems.

TEMIC is committed to providing cost-efficient, technically excellent solutions.

Digital Integration

Full Custom Designs Optimize Expertise Share: System/Customer and Integration/TEMIC

Full Custom Designs Handled by The Customer

- ○ Design completed by customer using TEMIC design rules, electrical rules and ESD protection, after Non-Disclosure Agreement sign-off.
- ○ Available processes are listed on page 1.2.
- ○ Customer supplies GDSII tape after DRC and LVS and test vectors according to TEMIC rules.
- ○ TEMIC delivers probed wafers, dice or package and tested parts. Test is done on TEMIC digital tester.
- ○ Warranty is limited to final test according to customer test vectors.

Full Custom Designs Handled by TEMIC

After agreement on the required specification is reached between the customer and TEMIC, the design is fully completed by TEMIC from specification to final post-layout simulation. TEMIC will ask for customer agreement on specific items or for final simulation results before wafer processing.

All BiCMOS designs are handled as Full Custom Designs whatever the physical implementation.

Full Custom offering is a turnkey solution proposed by TEMIC to develop optimized circuits for cost sensitive, medium complexity CMOS ASICs with high production volume.

Automated Custom can mix any TEMIC physical implementation Arrays, Composite Arrays, Cell Based and Full Custom “A LA CARTE” blocks.

TEMIC will use its system expertise in different applications. For example:

- ○ Automotive: Dash Board Controller
  Network Protocol Controller
- ○ Telecom: PLL
  IQ Modulator
  V110, V120 Protocol Controller
  ATM/SDH Interface Up to 622 MHz
- ○ Computer: Tag ASICs

Using every available CMOS process TEMIC offers optimized solutions for digital integration.

BiCMOS Designs

Due to the fact that high speed is the key feature of BiCMOS processes, TEMIC can develop designs on a turnkey basis using predefined Gate Arrays, or pure Full Custom Designs.

Electrical simulation is necessary. TEMIC will optimize speed, high sink or source current, noise immunity, and/or packaging in compliance with customer request.

0.8- m BiCMOS Gate Array

Description

MF is a high speed gate array combining 10-GHz n-p-n bipolar transistors, with CMOS 0.8- m, two metal layer technology. Mixing bipolar and CMOS devices in unit circuits of ASICs, TEMIC BiCMOS technology provides both speed performances compatible with bipolar LSIs and integration close to that of CMOS LSIs, keeping low power competitiveness.

TEMIC can develop MF designs on a turnkey basis.

Features

- BiCMOS technology – CMOS 0.8- m, two metal + n-p-n bipolar transistor
- High level of utilisation
  - Up to 85%
- Large range of operating modes:
  - CMOS/TTL/PSEUDO ECL . . . . . (0 – +5 V)
  - ECL . . . . . (–5 V – 0)
  - Mixed mode . . . . . (–5 V – 0 – +5 V)
- High speed performance:
  - CMOS NAND2 typical delay: 0.44 ns (FANOUT 4- - -)
  - BiCMOS NAND2 typical delay: 0.29 ns (FANOUT 4- - -)
  - TTL input buffer delay : 0.95 ns (FANOUT <= 10)
  - 32 mA TTL fast output buffer: 1.3 ns (LOAD: R = 390 µ , C = 50 pF)
  - 32 mA ECL output buffer: 0.75 ns (LOAD: R = 50 µ , C = 50 pF)
- Flexible I/O configuration: input, output, three-state, bi-directionnal, V_{CC}, GND, V_{EE}
- Three output buffer options: fast, normal, low noise
- 10-K, 100-K ECL standards supported
- Programmable output drive from 3.2 to 40 mA (SINK, SOURCE), parallelism up to 64 mA
- Optional D-latch in each I/O
- Dedicated software for optimum memory integration
- Class 2 and latch-up free
- Max toggle frequency: 500 MHz

Product Outline

Type	Total Gates	Max Estimated Usable Gates**	Maximum Programmable I/O
MF5K	5220	4700	76
MF13K	13536	12100	120
MF32K	32832	26300	186
MF50K	50196	37700	232
MF92K*	92232	64500	316

* On request.
** Depending on the application.

I/O Flexibility

TEMIC BiCMOS gate array concept can cope with CMOS/TTL requirements as well as ECL and PSEUDO-ECL interfacing.

The peripheral basic cell was built to guarantee the right POWER SUPPLY implementation next to any I/O type:

- V_{CC} and GND, or GND and V_{EE} for CMOS/TTL or ECL interfaces
- V_{CC}, GND and GND, V_{EE} in case of mixed mode (two supplies are needed).

Inputs

Each input can be programmed as CMOS, TTL, PSEUDO-ECL, ECL classical interface. SCHMIDTT TRIGGER with or without PULL-UP/PULL-DOWN resistor are also available for CMOS/TTL applications.

Outputs

From a single output buffer, CMOS, TTL, PSEUDO-ECL drives are available.

For switching noise and power consumption reduction, CMOS and TTL outputs, provide slew-rate and current drive adjustment facilities.

Current drive capacities are 12, 24, 32, 40 mA (64 mA available with parallelism).

SLEW RATE is controlled by different resistor values within three buffer types:

- Fast output buffer
- Normal output buffer
- Low noise output buffer

As a matter of fact, the intrinsic propagation delay is increased while reducing the noise.

ECL 10-K and ECL 100-K standards are supported by dedicated buffers. Beware of ECL 100-K standard definition which doesn't obviously fit with military specifications.

Power Supply Requirements

To provide clean supplies rails to all parts of the matrix, and for a better current density control, three different areas are isolated:

- the CORE
- the QUIET PART of the buffers (close to the core)
- the POWER PART of the buffer (close to the pad)

Absolute Maximum Ratings

Ambient temperature under bias (T_A)
Commercial . . . . . 0°C to +70°C
Industrial . . . . . –40 to +85°C
Military . . . . . –55 to +125°C
Maximum Junction Temperature . . . . . 150°C
Storage Temperature . . . . . –65 to + 150°C
TTL/CMOS :
Supply Voltage V_{CC} . . . . . –0.5 V to +7 V
I/O Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

ECL :
Supply Voltage V_{EE} . . . . . +0.5 V to –7 V
I/O Voltage . . . . . +0.5 V to V_{EE} – 0.5 V

Stresses at or above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

AC Characteristics Example (T_A = 25°C)

Specified at V_{CC} = +5 V when CMOS/TTL and V_{EE} = –5 V when ECL

Symbol Type	Macro	Description	Typical Propagation Delay (ns) Fanout			
			2	4	6	8
CMOS t_P BiCMOS t_P	NAND2	2-input NAND	0.33 0.24	0.44 0.29	0.55 0.33	0.64 0.36
CMOS t_P D2QWh CK	DFFR1	D Flip-Flop with positive Reset	0.89	1.10	1.27	1.45
t_{PLH} t_{PHL}	BUFINMOS	CMOS input Buffer	0.54 0.48	0.56 0.51	0.57 0.52	0.59 0.54
t_{PLH} t_{PHL}	BUFINTTL	TTL input Buffer	0.82 1.05	0.84 1.07	0.85 1.08	0.86 1.12
t_{PLH} t_{PHL}	BUFINECL	ECL input Buffer	0.71 0.82	0.72 0.82	0.73 0.85	0.76 0.88
ns			1 Supply	2 Supplies	LOAD	
t_P	BU...	fast TTL buffer normal TTL buffer low noise TTL buffer	1.30 2.45 6.20	2.25 3.45 7.15	50 pf, 390 µ 50 pf, 500 µ 50 pf, 500 µ	
t_P	BU...	fast CMOS buffer normal CMOS buffer low noise CMOS buffer	1.50 2.60 6.35	2.35 3.65 7.35	50 pf, 390 µ 50 pf, 500 µ 50 pf, 500 µ	
t_P	BU...	ECL 10-K buffer ECL 100-K buffer	0.75 0.75	0.75 0.75	15 pf, 50 µ 15 pf, 50 µ	

Ordering Information

Consult your TEMIC sales office.

Radiation-Tolerant 0.8-µm BiCMOS Gate Arrays

Description

TEMIC/Matra MHS is the first European supplier for space application submicron radiation tolerant gate arrays.

This is why TEMIC keeps offering a wide range of quality levels and makes space/radiation tolerant capability available on its advanced submicron BiCMOS MF gate arrays family. The mask compatible space/radiation tolerant process, called "MFRT," is a result of the TEMIC "Dual Use Technology" strategy serving the AMS (Avionics, Military and Space) market segments.

It allows the user to either go directly to radiation tolerant prototypes and flight models delivery, or to start with cheaper non radiation tolerant prototypes. The user can then convert to a radiation tolerant version, only when EQM or FM are actually needed, provided proper simulations have been run before choosing either solution.

TEMIC can develop MFRT designs on a turnkey basis.

Features

- Mask compatible radiation tolerant version of the MF gate arrays family
- No rebound effect demonstrated after annealing
- Total dose capability evaluated on a design basis
- Positive influence of space very low dose rate (< 1 rad/h) expected
- Latch-up free: better than 100 MeV
- SEU threshold better than 50 MeV
- Suitable for most space projects, LEO, GEO or POLAR orbits and deep space,
- Advance very low power 0.8-µm BiCMOS process
- Total dose effect simulation through Kd
- Dedicated space design rules checkers

Basic Flow

The MFRT design flow follows the standard MF one, with specific space design rules which can be verified with dedicated space design rules checkers.

The simulation tools allow users to verify that under any level of total dose up to 85 Krad, the functionality and the speed performances are still met.

When the ASIC is to be procured at quality grades as MIL-STD-883 class S or SCC9000 level B, then a restriction shows up because of the die size, limiting the use of matrices to the MF50KE (the E stands for the RT version), at the best.

The package offering takes advantage of what has been set for the MCRT and is as follows:

- multi layers quad flat package with up to 256 pins, J, gull wing or flat leaded,
- side brazed technology with up to 64 pins.

So as to allow efficient design flow at both component and system levels, TEMIC has set an efficient route from the prototyping for A or B models, to flight models representative for EQM, delivering.

After negotiation, TEMIC can also offer a full service for:

- either a radiation evaluation on a batch per batch basis,
- or a radiation lot acceptance test (RLAT)

Finally, and as a natural consequence of our "dual use technology," for the purpose of better silicon usage efficiency and better performances, our composite MFM offering is also available for space applications with the same features and capabilities as our "MFM" and "MFRT" as a full custom.

Propagation Delay Factors

Propagation delays are a function of several factors, including fanout, interconnection capacitance, supply voltage, junction temperature, and process tolerance.

To convert nominal delay values (V_{CC} = 5 V, T_A = 25°C, Typical process), into worst case values, apply derating coefficients Kp, Kv, Kt, which are displayed below.

Process
$0.7 < k_p < 1.4$

Voltage	KV
4.50 V	1.09
4.75 V	1.04
5.00 V	1.00
5.25 V	0.95
5.50 V	0.89

Temperature	KT
–55°C	0.80
–40°C	0.84
0°C	0.91
25°C	1.00
75°C	1.09
125°C	1.21

Packaging

TEMIC offers a wide range of packaging options including CPGA, CQFP, SOIC, PLCC, CLCC, QFP, Wafer, Dio. For BiCMOS devices, packaging must be chosen according to speed and power consumption specification.

TEMIC also offers optimal associations, package/BiCMOS MATRIX for power dissipation control and thermal management.

These associations were checked by thermal simulations, taking care of the maximum accepted junction temperature, and the context of the application (temperature, air speed, thermal exchanges, etc.).

Type	MF5K	MF10K	MF32K	MF54K	MF92K	Pins
Copper lead frame PQFP	100	128	160	240	304 on request	”
MQUAD (R)	_	128	208	240	on request	”
Heat sink MQUAD (R) down		128 *	208 *	240 *	on request	”
Alumina cerquad	100	132/JEDEC 128/EIAJ	196/JEDEC *	240	304 on request	” ”
Multilayer Alumina quad pack	CLCC 84	132/JEDEC	196/JEDEC	256/JEDEC	348/JEDEC	”
Heat sink multilayer Alumina quad pack	_	on request	on request	on request	on request	”
Alumina PGA	100	144	209	299	340 D	”
Heat sink Alumina PGA	on request	144 D	207 D *	300 D	340 D	”

(R) Registered Product of olin
* Special pattern

It is mandatory before final package selection, to compute power consumption calculation, and check with TEMIC offices, the right package solution.

0.8-µm BiCMOS Composite Gate Arrays

Description

TEMIC, taking advantage of being a standard ICs manufacturer (SRAM, DPRs, FIFOs,...) bridges the gap between full custom designs and gate arrays with its "Composite" concept, offering the possibility to merge hard blocks into arrays of standard spare gates, to create:

- faster speed,
- lower power consumption,
- higher density, preventing from design partitioning,

Our MFM 0.8-µm BiCMOS composite gate arrays offer the best trade off between low design cost and short prototyping cycle time, and high integration density.

TEMIC can develop MFM designs on a turnkey basis.

Features

- advanced very low power 0.8-µm BiCMOS process
- allows high level of local integration and high speed performances with :
- mega blocks from customers or TEMIC libraries
- COMPASS compiled blocks (two port RAM, data path,...)
- TECHGEN for RAM and ROM generation

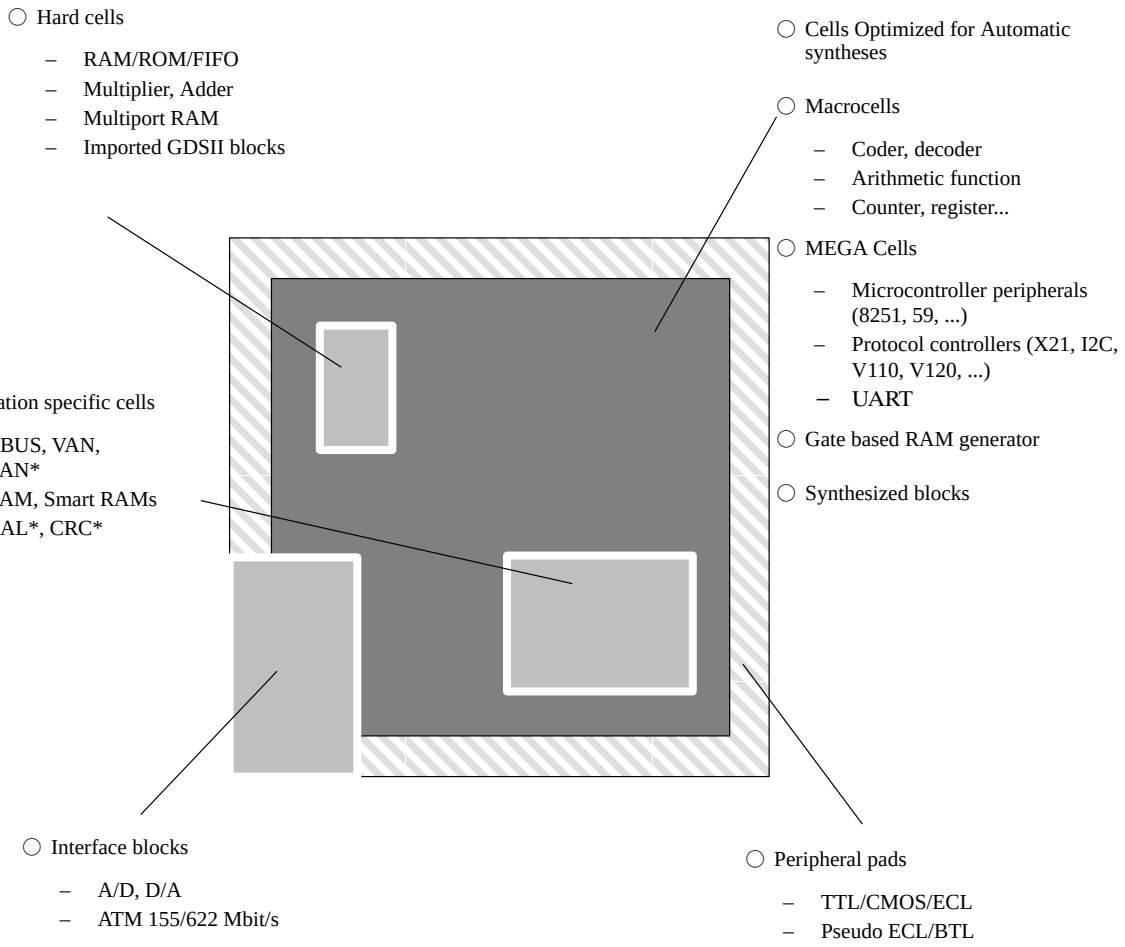
Basic Flow

The MFM design flow follows the standard MF ones, but as a full custom service, once one has defined the blocks and the number of spare gates with their floor plan, the user operates as with a standard gate array. If the content of the array has been agreed before the design is completed and signed off, TEMIC manages to process the first steps of the silicon process, allowing to start immediately the metallization layers once design is signed off.

The package styles offered is similar to the MF offering.

Finally, and as a natural consequence of TEMIC "dual use technology," the composite MFM offering is also available for space applications with the same features and capabilities as our "MFM" and "MFRT," but as a full custom service.

0.8-µm BiCMOS Composite Array



* under development

Customer and TEMIC Design Flows

Design Offering

Five different ASIC design offerings are available: ULC, Gate Arrays, Composite Arrays, Cell Based and Full Custom. Each physical implementation gives an answer to the compromise: flexibility/unit price and integration/development cost.

Design Modes

Three different design modes can be agreed upon between the customer and TEMIC, depending on system and integration skills requirements.

Mode	Logic Design	Physical Layout	Design Tools
Customer Design	Customer	Customer	Customer tools
Customer and TEMIC Design	Customer	TEMIC	TEMIC supported tools[a] (Netlist and simulation)
TEMIC Design	TEMIC	TEMIC	TEMIC supported tools[a] (Netlist and simulation)

a. Supported tools are currently CADENCE, COMPASS, MENTOR, SYNOPSYS and VHDL/VITAL.

Design Modes versus Design Offering

Mode / Product Family	Customer Design	Customer and TEMIC Design	TEMIC Design
ULC			□
Gate Array		x	□
Composite Array		x	□
Cell Based	x	○	□
Full Custom	x		□

x : standard offer.
○ : dependant on human and hardware resources needed and/or available.
□ : specific development using TEMIC own expertise.

Design Phases and Meetings

The design of a circuit is separated into four main phases, separated by three major meetings between TEMIC and the Customer, as shown in Figure 1.

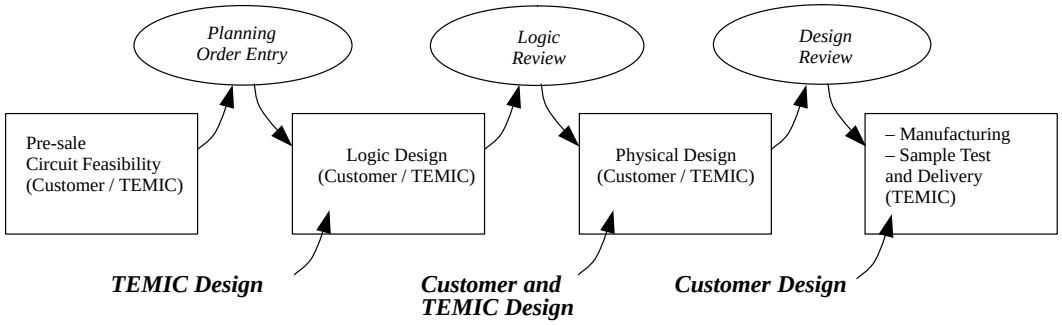


Figure 1. The Design Phases and Meetings

Technology for Digital Integration

Description

TEMIC develops a wide range of CMOS technologies, used for catalog products or ASICs' in volume production. Their common features are high performance/high speed both with low power consumption, either in stand-by or operating modes.

TEMIC makes these technologies available for selected customers/partners for their own design.

Features

TEMIC technologies include digital CMOS technologies and several derivatives from the CMOS core basis:

- mixed analog/digital series with one more polysilicon layer and low V_t transistors
- non-volatile series with high voltage NMOS transistors and programming/sensing/erasing capabilities
- radiation tolerant process with specific guard rings

	Technology	Well	Lithography (µm)	Poly Layers	Metal Layers	Operating Voltage (V)	Characteristics
Digital Series							
FCC1D	CMOS	N	0.8	1	2	5 or 3	
FCC1S	CMOS	N	0.8	1	1	5 or 3	
FCC2D	CMOS	Twin	0.6	1	2	5 and/or 3	
FCC2T	CMOS	Twin	0.6	1	3	5 and/or 3	
FCB1D	BICMOS	Twin	0.8	1	2	5 and/or 3	NPN
Mixed Analog/Digital Series							
FCA1D	CMOS	N	0.8	2	2	5 and/or 3	Low V_t
FCA2D[a]	CMOS	N	0.6	2	2	5 and/or 3	
FCA2T[a]	CMOS		0.6	2	3	5 and/or 3	
Non Volatile Series							
FCN1D	CMOS	2	0.8	1	2	5	EPROM
FCN2T[a]	CMOS	2	0.6	1	3	5 and/or 3	EPROM
Radiation Tolerant Series							
FCT1D	CMOS	N	0.8	1	2	5	Guard Ring
FCBTD	BICMOS	Twin	0.8	1	2	5	Guard Ring
FCT2D	CMOS	Twin	0.6	1	3	5 and/or 3	Guard Ring

a. Planned